REMARKS

Claims 1-18 are pending in the application and stand rejected.

Rejection under 35 U.S.C §102

Claims 1, 3-10, 12-15, 17 and 18 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,589,067 to Porter et al. In particular, the Examiner finds that, with regard to claim 1, Porter discloses all of the claimed limitations.

In the previously submitted reply, Applicants noted that Claim 1 is directed to a computer system having first and second processors wherein the second processor consumes instructions derived from the first processor through a decoupling element, and that in the system of Porter, on the other hand, the floating point vector processor (i.e. the second processor) does not consume instructions derived from the host computer (i.e. the first processor). Porter describes three modes of operation of the system 10 (i.e. the second processor): a tightly-coupled mode, a loosely-coupled mode, and an uncoupled mode. In the tightly-coupled mode the vector processor 10 is interfaced to the host computer and "software, resident in the host, controls system data acquisition, function evaluation in the pipeline and output data writes to the host". In the loosely-coupled mode the vector processor downloads and then operates on data received through I/O ports. In the stand-alone mode software resident internally in the vector processor is used for function evaluation and data input/output. Thus, the different coupling modes differ solely in the manner by which software become available to the vector processor (and hence how it is accessed by the master processing unit 12 of the vector processor). Once this software is made available, the function of the vector processor with respect to the host computer is the same (col. 4, l. 54-) and it consists of performing "computationally intensive functions" on *data* received from the host computer. Thus, the vector processor does not receive instructions from the host computer but rather only receives data upon which it performs preprogrammed algorithms or functions.

In the final Action, the Examiner asserts that Porter does indeed describe a system wherein the vector processor consumes instructions from the host processor by virtue of the host

processor passing data to the vector processor, thereby instructing the vector processor which data to use. Applicants respectfully note that this is clearly not anticipatory of claim 1, because claim 1 clearly recites that the second processor receives data from and writes data to the memory, and thus does not receive data from the first processor as per Porter. To make clear that the instructions received from the first processor are not data, Applicants have amended the claims to recite that the second processor receives computations from the first processor and then executes these computations decoupled from the first processor. Applicants submit that claim 1, as amended, clearly reads over Porter because Porter does not pass computations to the vector processor but rather passes data to the vector processor upon which computations already resident in the vector processor are then performed. Applicants thus respectfully urge the Examiner to allow claim 1 as amended herein.

Claims 3-10, 12-15 and 17 depend from claim 1. In view of the above discussion, it is submitted that claim 1 is allowable, and for this reason claims 3-10, 12-15 and 17 are also allowable.

Claim 18 is a method claim that corresponds to apparatus claim 1 and that includes the step of passing instructions to a second processor for executing a task. As elaborated upon above, this is a different method of operating than that disclosed by Porter, wherein only data (not instructions) is passed to the vector processor for processing thereof. Applicants note with particularity that claim 18 recites identifying part of a code as providing a task to be carried out by the second processor, and then passing information defining the task to a decoupling element, which then passes instructions derived from this information. Applicants understand and appreciate the Examiner's view of the disclosure of Porter, as further elaborated upon in the final Action, but respectfully submit that even when taking this view, the passing of data from the host processor to the vector processor to be acted upon by computations already resident in the vector processor cannot possibly be understood as being the same as passing instructions derived from information that defines a task to be carried out. Applicants respectfully submit that there is no basis in the art, in the present application, or in the prior art to understand that a task to be carried out is or can be the same as data to be operated on. Thus, Applicants respectfully submit that this claim, as presently pending, is also novel and allowable over Porter.

Rejection under 35 U.S.C §103

Claims 2, 6, 11 and 16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Porter in view of U.S. Pat. No. 6,237,079 to Stoney or the Hennessy article. Claims 2, 6, 11 and 16 depend from claim 1. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, in light of the above discussion of claim 1, we submit that claims 2, 6, 11 and 16 are also allowable.

In view of the above, we submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 08-2025. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 08-2025.

I hereby certify that this correspondence is being deposited with the United States Post Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

March 23, 2005
(Date of Transmission)

Corinda Humphrey
(Name of Person Transmitting)

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3-23-05
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